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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/726,380	GABRIEL ET AL.
	Examiner	Art Unit
	Long K. Tran	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amdt on January 20, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 28-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 28-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to Amendment filed on January 20, 2006.

2. Claims **4, 7 – 27** have been cancelled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1, 2** and **5** are rejected under 35 U.S.C. 102(e) as being anticipated by En et al. (US Patent No. 6,764,966).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

5. Regarding claim **1**, En discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer 20 (figs. 1 – 5; step S54; column 8, lines 60 – 67) on a semiconductor substrate 12 (figs. 1 – 6);

forming a gate electrode 18 (figs. 1 – 6; column 8, lines 63 – 67) over the gate dielectric layer (20) wherein the gate electrode (18) defines a channel interposed

between source/drain regions 14/16 (figs. 1 – 6) formed within an active region of the semiconductor substrate (12); and

forming contact etch resistant spacers 26 (figs. 1 – 6; column 9, lines 30 – 39) on sidewalls of the gate electrode (18) and sidewalls of the gate dielectric layer (20), the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material (Al_2O_3; column 5, lines 26 – 67 and column 6, lines 16 – 18); and

forming liner layer 28 (figs.1 – 6; Step S58; column 5, lines22 – 26 and column 9, lines 41 – 49) over the contact etch resistant spacers (26) of Si_3N_4.

Regarding claim **2**, Kim discloses forming the contact etch resistant spacers (26) includes the steps of:

forming a contact etch resistant layer on the sidewalls of the gate electrode (18), the sidewalls of the gate dielectric (20) and portions of the upper surface of the semiconductor substrate (12). See (figs. 2 – 5); and

etching the contact etch resistant layer to form the contact etch resistant spacers (fig. 1; Step S62; column 10, lines 36 – 44).

Regarding claim **5**, Kim discloses forming a silicon-oxide interlevel dielectric layer 32 (fig. 6; column 9, lines 59 – 67).

6. Claims **28** and **29** are rejected under 35 U.S.C. 102(e) as being anticipated by Honeycutt et al. (US Patent No. 6,734,071).

7. Regarding claim **28**, Honeycutt discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer 22 (figs. 1 – 9) on a semiconductor substrate 12 (figs. 1 – 9);

forming a gate electrode 24/26 (figs. 1 – 9) over the gate dielectric layer (22) wherein the gate electrode (24/26) defines a channel interposed between source/drain regions 34/36 (figs. 1 – 9) formed within an active region of the semiconductor substrate (22); and

forming spacers 102 (figs. 7 – 9) on sidewalls of the gate electrode (24/26, the spacers having etch selectivity with respect to silicon oxide and silicon nitride material (Al_pO_q; column 6, lines 5 – 12);

forming a contact mask over the interlevel dielectric layer 62 (figs. 8 – 9) and etching a contact aperture 66, 68, 70 (fig. 9; column 6, lines 21 – 33) to expose a source/drain region 50 (fig. 9); and filing the contact aperture with a conductive material 72 (fig. 9) to form a contact that is electrically coupled to one of the source or drain and is electrically isolated from the gate electrode, the contact touching the spacer in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode.

Regarding claim **29**, Honeycutt discloses forming the spacers includes:

Forming a spacer material 102 (fig. 6) on the sidewalls of the gate electrode (24/26), the sidewalls of the gate dielectric (22) and portions of the upper surface of the semiconductor substrate (12); and

Etching the spacer material to form the spacers (fig. 7; column 6, lines 14 – 18).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **1, 2, 3, 5** and **6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US Patent no. 6,137,126) in view of in view of Hagemeyer et al. (US Patent Application Publication No. 2006/0008959).

10. Regarding claim **1**, Avanzino discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer 14 (fig. 1) on a semiconductor substrate 12 (fig. 1);

forming a gate electrode 16 (fig. 1) over the gate dielectric layer 14 wherein the gate electrode 16 defines a channel interposed between source/drain regions 13/13' (fig. 1) formed within an active region of the semiconductor substrate; and

forming contact etch resistant spacers 20 (fig. 1) on sidewalls 15 (fig. 1) of the gate electrode16 and sidewalls of the gate dielectric layer 14, the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material (SiC; column 3, lines 59 – 67 and column 4, lines 1 – 8 and lines 43 – 46).

Avanzino does not teach forming liner layer over the contact etch resistant spacers of at least one of Si_xN_y and SiO_xN_y.

However, Hagemeyer shows a silicon nitride liner 217 over a contact etch resistance layer 215 when wet-chemical etching process in used ([0099]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Avanzino's device with a silicon nitride (Si_xN_y) liner over the contact etch resistance as shown by Hagemeyer in order to provide an wet etch of the sidewall being guaranteed to stop with sufficient reliability ([0099]).

Regarding claim **2**, Avanzino discloses forming the contact etch resistant spacers 20 includes the steps of:

forming a contact etch resistant layer (not shown; column 4, lines 37 – 43) on the sidewalls 15 of the gate electrode 16, the sidewalls 15 of the gate dielectric 14 and portions of the upper surface (not labeled) of the semiconductor substrate12; and

etching the contact etch resistant layer to form the contact etch resistant spacers 20 (column 4, lines 43 – 46).

Regarding claim **3**, Avanzino discloses forming the contact etch resistant layer of at least one of silicon carbide.

Regarding claim **5**, Avanzino discloses forming silicon oxide inter-level dielectric layer 21 (fig. 1; column 2, lines 60 – 61 and column 4, lines 35 – 36) over the contact etch resistant spacers 24.

Regarding claim **6**, Avanzino discloses etching a contact aperture or opening in the inter-level dielectric layer 21 exposing a source/drain (column 2, lines 62 – 63).

Avanzino does not explicitly shows a step of forming a contact mask over the inter-level dielectric layer 21.

However, it is known in the semiconductor technology that to etch a dielectric layer for forming an aperture or opening therein, one partisan in the art would forming a

contact mask over the inter-level dielectric layer, patterning the contact mask layer (imaging and developing) then etching the inter-level dielectric layer. Reference to Uehara et al. (US Patent No. 6,713,826; mask 74 (fig. 5(d)); column 11, lines 59 – 67) is cited for the purpose of showing this fact, but not used in the rejection. Thus Avanzino process of fabricating a semiconductor device reads on the claimed forming a contact mask over the inter-level dielectric layer.

11. Claims **28, 31** and **33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US Patent No. 6,479,359) in view of Honeycutt et al. (US Patent No. 6,734,071).

12. Regarding claims **28** and **31**, Kim discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer 22 (figs. 3A) on a semiconductor substrate 21 (fig. 3A);

forming a gate electrode 23 (figs. 3A – 4D) over the gate dielectric layer 22 wherein the gate electrode 23 defines a channel interposed between source/drain regions 26 (figs. 3A – 4D) formed within an active region of the semiconductor substrate 21; and

forming spacers 24/25 (figs. 3C, 3D, 4C and 4D) on sidewalls of the gate electrode 23 and sidewalls of the gate dielectric layer 22, the spacers having etch selectivity with respect to silicon oxide and silicon nitride material (tungsten/polysilicon; column 5, lines 8 – 14; metal ; column 3, lines 8 – 40);

Kim does not teach forming a contact mask over the interlevel dielectric layer and etching a contact aperture to expose a source/drain region; and filing the contact aperture with a conductive material to form a contact that is electrically coupled to one of the source or drain and is electrically isolated from the gate electrode, the contact touching the spacer in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode

However, Honeycutt teaches forming a contact mask over the interlevel dielectric layer 62 (figs. 8 – 9) and etching a contact aperture 66, 68, 70 (fig. 9; column 6, lines 21 – 33) to expose a source/drain region 50 (fig. 9); and filing the contact aperture with a conductive material 72 (fig. 9) to form a contact that is electrically coupled to one of the source or drain and is electrically isolated from the gate electrode, the contact touching the spacer in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for forming an interlevel dielectric layer over the liner, forming a contact mask over the interlevel dielectric layer and etching a contact aperture to expose a source/drain region, filling contact aperture with conductive (metal) layer of Kim's as taught by Honeycutt in order to electrically contact the FET to the other parts of the device.

Regarding claim **33**, Kim and Lee disclose including forming a silicon oxynitride liner layer 52 (Lee, figs. 6 and 7; column 1, line 28 – 32 (reference to Zhou et al., US

Patent No. 5,930,627); and column 3, lines 51 – 55) between the spacers 50 and the interlevel dielectric Layer 70.

13. Claims **28 – 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US Patent no. 6,137,126) in view of Lee et al. (US Patent no. 6,372,569).

14. Regarding claims **28** and **30**, Avanzino discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer 14 (fig. 1) on a semiconductor substrate 12 (fig. 1);

forming a gate electrode 16 (fig. 1) over the gate dielectric layer 14 wherein the gate electrode 16 defines a channel interposed between source/drain regions 13/13' (fig. 1) formed within an active region of the semiconductor substrate;

forming spacers 20 (fig. 1) on sidewalls 15 (fig. 1) of the gate electrode16 and sidewalls of the gate dielectric layer 14, the spacers are SiC having etch selectivity with respect to silicon oxide and silicon nitride material (SiC; column 3, lines 59 – 67 and column 4, lines 1 – 8 and lines 43 – 46);

forming a silicon oxide interlevel dielectric layer 21 over gate electrode and the spacers.

Avanzino does not teach forming a contact mask over the interlevel dielectric layer and etching a contact aperture to expose a source/drain region; and filing the contact aperture with a conductive material to form a contact that is electrically coupled to one of the source or drain and is electrically isolated from the gate electrode, the

contact touching the spacer in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode. In other words, Avanzino does not teach forming a contact via for contacting the source and drain of the FET to other parts of the device for the FET to function.

However, Lee teaches forming a contact via (92/96, Fig. 7) for contacting the source and drain 36 of the FET to other parts (not shown) of the device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Avanzino's process such that it includes forming a contact via. One would have been motivated to make such a change in view of the teachings in Lee that such a change allows the FET to contact other parts of the device, for the device to function.

Such modification, i.e., adding the missing via contact, would require necessary steps including ..... More specifically, such modification would result in:

forming a contact mask (as taught by Lee, as mentioned above) over the interlevel dielectric layer (21, Avanzino);

etching a contact aperture (90 or 92, Fig. 7, Lee) to simultaneously expose one of the source or the drain (13 or 13', Avanzino) and at least a portion of an adjacent spacer (42/52); and

filling the contact aperture with a conducive material (96) to form a contact that is electrically coupled to the one of the source or drain (as is clearly seen from Fig. 7) and is electrically isolated from the gate electrode (16, Fig. 1, Avanzino), the contact touching the spacer (42/52, Lee, as required in the process of forming the contact

taught by Lee) in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode.

Regarding claim **29**, Avanzino discloses forming the spacers includes:

forming a spacer material layer on the sidewalls of the gate electrode, the sidewalls of the gate dielectric and portions of the upper surface of the semiconductor substrate; and etching the spacer material layer to form the spacers 20 (Avanzino; fig. 1; column 4, lines 5 – 14).

Regarding claim **31**, Lee discloses the spacers comprise undoped silicon (column 3, lines 43 – 47).

Regarding claim **32**, Lee discloses forming a silicon nitride liner layer 52 (figs. 5 – 7; column 3, lines 51 – 55) between the spacers (42/50) and the interlevel dielectric layer 70 (figs. 5 – 7).

Regarding claim **33**, Kim and Lee disclose including forming a silicon oxynitride liner layer 52 (Lee, figs. 6 and 7; column 1, line 28 – 32 (reference to Zhou et al., US Patent No. 5,930,627); and column 3, lines 51 – 55) between the spacers 50 and the interlevel dielectric Layer 70.

Regarding claim **34**, Kim and Lee disclose the claimed invention of claim 28 and the spacer is about 135Ă to 165Ă instead of between 200Ă and 400Ă as cited in the instant claim.

However, it would have been well known in the art that the selection of those parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, range, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, range, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

Regarding claim **35**, Kim and Lee disclose forming a silicon nitride dielectric liner layer between the spacers and the interlevel dielectric layer, and the etching a contact aperture Includes etching a portion of the interlevel dielectric layer and a portion of the liner layer (Kim, fig. 7; column 4+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

February 27, 2006